

Nano-meter scale heterogeneous III-V semiconductor-silicon photonic integration

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It is pointed out that the fully recognised and ever growing need for a combination of photonic and electronic functionalities could be made fully effective by the heterogeneous integration of active III-V semiconductor/passive silicon photonics and silicon microelectronics. It is shown that the inevitable scaling down to nano-meter range of photonic integration requested by the necessary matching to microelectronics is made possible by the heterogeneous association of III-V semiconductor and silicon membranes including high index contrast and nano-meter scale structuring. It is emphasized that these membrane photonic nanostructures can be considered as the absolute must on the track to the ultimate confinement of photons which is highly desired in the prospect of the development of micro-nano-photonic devices and systems. Examples of devices and systems along this approach are presented (micro-laser/micro-guide integration, active devices with very low threshold etc.). [DOI: 10.2971/jeos.2008.08024]

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1 INTRODUCTION: THE NEED FOR HETEROGENEOUS MICRO-NANO-PHOTONIC INTEGRATION

The continuous growth of system complexity makes it inevitable the development of technological schemes where different material systems, device families are heterogeneously integrated to take full advantage of the variety of functional combinations, while decreasing the cost of the fabrication process, both in time and consumption and easing the interconnections between the various available functionalities.

In that respect, it has become increasingly recognised that the combination of photonic and electronic functionalities could be made fully effective by the heterogeneous integration of active/passive photonic and silicon microelectronic circuits. Figure 1 shows a schematic illustration of photonic integration with micro-electronics. In this particular so called "above-IC" integration scheme, a photonic layer is formed on top of the microelectronic circuits.

This approach is presently generally adopted when it comes to combine, at the *microelectronic chip level*, photonic and electronic functionalities. The most popular recent developments along this line concern the use of the photonic functionality as a high bit rate and "long range" interconnect level, necessary to circumvent the inevitable limitations inherent to metallic interconnections. However photonic functionality is not bound to this particular somewhat trivial, yet very important,

application and is expected to evolve into complex systems on chip.

The reader will have understood that, in this general context of photonic-microelectronic integration, the requested nano-meter scale of photonic integration is dictated by the necessary topological and size matching with micro-electronic circuits. This is not, however, the sole driving force for photonic miniaturisation. Another important aspect lies in the energetic-thermal budget of the photonic integrated system: the ability to *confine* photons within tiny volumes is essential

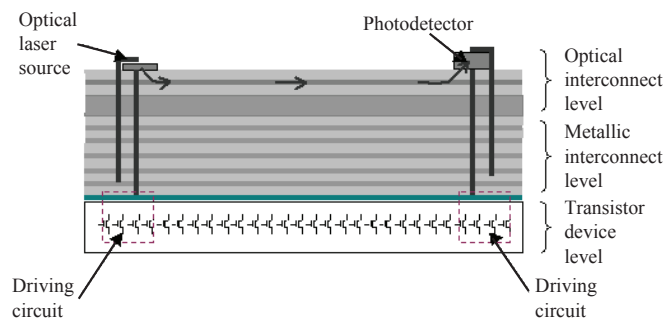


FIG. 1 Schematic representation of the so called above IC photonic-microelectronic heterogeneous integration.

for the efficient operation (that is to say at low energetic cost) of a wide range of active micro-nano-photonic devices, including low threshold micro-lasers [1]-[3] and non-linear optics devices [4].

In the next section, it is argued that photon confinement schemes based on high index contrast nano-structured semiconductor membranes provide the appropriate solutions to above mentioned requirements. It is further argued in Section 3 that the technology schemes to be adopted are compatible with technological approaches which are normally describable as planar and are familiar to the world of silicon micro-electronics. In Section 4, examples of recent achievements of heterogeneous active/passive III-V/silicon integration along this line are presented.

2 HIGH INDEX CONTRAST NANO-STRUCTURED SEMICONDUCTOR MEMBRANES: THE “MUST” FOR PHOTON CONFINEMENT

The principal objective of micro-nano-photonics lies in this simple definition: *the control or confinement of photons within the tiniest possible space during the longest possible time*. The general approach to meet this objective consists in high index contrast structuring of space at the wavelength scale, which is in the sub-micron range for the optical domain. Materials commonly in use for that purpose are metals and high optical index dielectrics. Metals have attracted considerable attention recently in the context of plasmonics: very strong spatial confinement of photons can be attained in plasmonic nano-structures, at the expense however of a limited resonance strength (or confinement time) as a result of metal induced optical losses, which are a serious draw-back in the prospect of photonic integration. We will concentrate here on high index dielectric, namely III-V semiconductors and silicon.

In the membrane approach, photons are confined “vertically” in planar and high optical index semiconductor waveguide membranes, surrounded by low index cladding materials (such as air/vacuum for suspended membranes [5, 6] or, for example, silica, for bonded membranes, as further described later). Strong refractive vertical confinement is achieved owing to the high contrast ratio of the vertical optical index profile.

In mono-mode operation conditions, the thickness of the membrane is very thin, around a fraction of μm ; it results that low loss coupling schemes with an optical fibre are not easily achievable, but, the positive counterpart lies in the relaxed technological constraints for the high index contrast lateral nano-structuring of the membrane. Also, the strong vertical confinement, leading to a reduced volume of the optical modes, lends itself to the production of very compact structures, which is essential for active devices to operate at the cost of very low injected power.

For the lateral confinement, two strategies are applied:

- Refractive confinement (as for vertical confinement), where use is made of the total or partial internal reflection of photons at the semiconductor-cladding interface, as schematically illustrated in Figure 2(a). This strategy, which is widely used in traditional optoelectronics, is principally devoted to devices operating solely in the wave-guided regime. Strong confinement of optical modes can be achieved along this approach, owing to the high index contrast between the confining semiconductor micro-structures and the surrounding cladding material (eg Si micro-guides, so-called micro-wires, or Si micro-rings shown in Figure 2(a)).
- Diffractive confinement (see Figure 2(b)): this is the world of photonic crystals. This strategy is not restricted to wave-guiding in plane operation, but may also apply to devices opened to the third direction of space and which are meant to communicate via diffraction phenomena with radiated modes accessible above the so called light cone. The concepts which underline the photonic crystal based confinement strategy are summarized below (and described in detail in [7]).

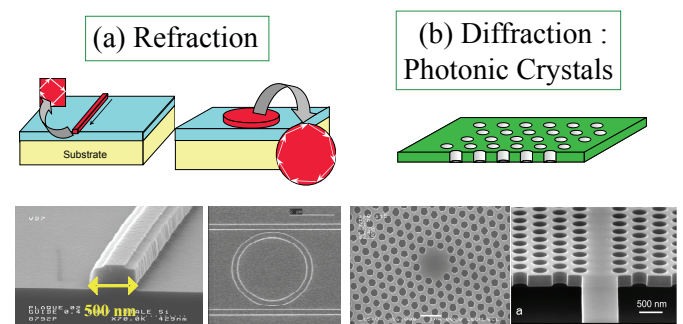


FIG. 2 Refraction (a) and diffraction (b) based confinement strategies.

A photonic crystal is a medium which the optical index shows a periodical modulation with a lattice constant on the order of the operation wavelength. The specificity of photonic crystals inside the wider family of periodic photonic structures, lies in the high contrast of the periodic modulation (generally more than that 200%): this specific feature is central for the control of the spatial-temporal trajectory of photons at the scale of their wavelength and of their periodic oscillation duration.

In photonic crystals, strong diffraction coupling between wave-guided modes occurs; these diffraction processes affect significantly the dispersion characteristics, or the so called band structure, according to the solid state physics terminology. The essential manifestations of these disturbances consist of (Figure 3):

- The opening of multidirectional and large photonic band gaps (PBG)
- The presence of flat photonic band edge extremes (PBE), where the group velocity vanishes, with low curvature (second derivative): $\alpha \cong 1/\text{PBG}$.

These are the essential ingredients which are the basis of the two optical confinement schemes provided by photonic crys-

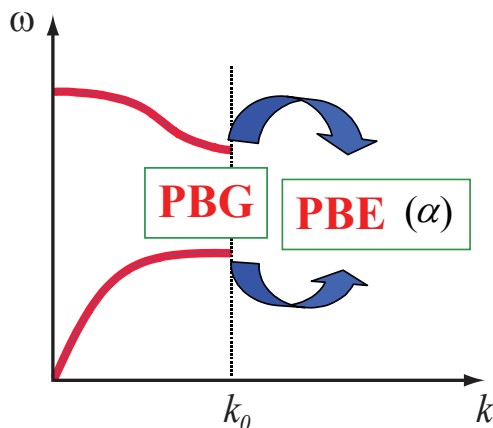


FIG. 3 Schematic representation of a photonic band gap (PBG) and of related photonic band edges (PBE) in the dispersion characteristics of a photonic crystal.

tals (PBG / PBE confinement schemes) and which make them the most appropriate candidates for the production of a wide variety of compact photonic structures.

In the PBG scheme, the propagation of photons is forbidden at least in certain directions. This is in particular true when they are trapped in a so called localized defect or micro-cavity and the related optical modes are *localized*: in this case the propagation of photons is fully prohibited. Opening of large PBG (in the spectral range) provided by the PC, allows for a very efficient trapping of photons, which can be made strongly localized in free space.

In the PBE scheme, the PC operates around an extreme of the dispersion characteristics where the group velocity of photons vanishes. It should be noted however that the dispersion characteristics apply strictly for infinite periodic structure and time and that the concept of zero group velocity is fully true only under these particular extreme conditions. The real common world is actually finite and transitory. It is therefore more appropriate to speak in terms of *slowing down* of optical modes (so called Bloch modes for a periodic structure), which remain however *de-localized*. It can be shown that the lateral extension of the area S of the slowing down Bloch mode during its lifetime τ is proportional to $\alpha\tau$ [3]. As mentioned above, one essential virtue of PC is to achieve very low curvature α at the band edge extremes, thus resulting in very efficient PBE confinement of photons.

The most efficient confinement of photons can be achieved with the PBG scheme. The PBE scheme provides weaker confinement efficiency than with the PBG approach, while resulting in an improved control over the directionality or spatial/angular resolution.

It should be mentioned, at this stage, that silicon is a very good photonic material: it is indeed an excellent photonic “conductor” for wavelengths beyond $1.1 \mu\text{m}$, where it is transparent, and owing to its high optical index. This is in particular true for the silicon on insulator (SOI) membrane configuration, where it forms (as for microelectronics) an ideal couple with the low optical index silica cladding; this configuration is fully available in the world of microelectronics. Silicon pos-

sesses, in addition, attractive non-linear characteristics (efficient two photon absorption, strong Raman gain coefficient etc.). An essential draw-back of silicon lies in its poor light generation characteristics, preventing its use as a gain material for laser emission, as this is readily achievable with III-V semiconductor materials.

In the next section it is shown that the membrane approach naturally lends itself, from the technological as well as conceptual view-points, to heterogeneous integration of active III-V optical devices with silicon based passive optical devices and microelectronics.

3 III-V/SILICON PHOTONIC HETEROGENEOUS INTEGRATION: PROMISING TECHNOLOGICAL PROSPECTS OF THE MEMBRANE APPROACH

The general approach which is deemed to be widely adopted for the photonic-microelectronic integration at the silicon chip scale consists in the bonding of the photonic layer on top of the microelectronic chip (above IC scheme). Among the various bonding techniques, the silica-silica molecular bonding procedure is presently the most advanced in terms of manufacturability. This technique is particularly well suited for the bonding of one or a few successive membrane semiconductor layers on a silica layer deposited on top of the silicon microelectronic chip and planarized. Not only do the different silica layers in between the semiconductor layers act as a low index optical “insulator”, but also they are integer part of the overall photonic structure; in that respect their thickness is a critical parameter of the design and has to be controlled carefully. This multi-membrane layer approach lends itself to active/passive III-V/silicon heterogeneous integration: it allows for a vertical separation of the active material (III-V) and passive (silicon) membrane layer levels.

In brief, this multi-level approach is not only meant to pile up several functional layers, but also, and more so, to open a realm of new functionality: this is allowed for by the optical interplay between the different layers.

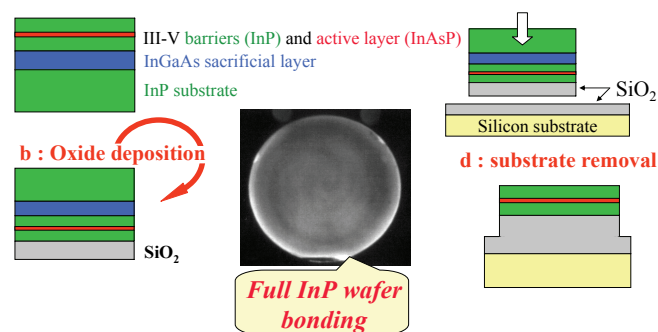


FIG. 4 Technological steps of the molecular bonding procedure.

Figure 4 shows the technological steps of the molecular bonding procedure illustrated in the case of an InP active membrane with InAsP quantum wells bonded onto silica on a silicon substrate (see for example [1], for a complete description

of the SiO₂-SiO₂ molecular bonding technological procedure, developed at CEA-LETI). The heterostructure, epitaxied on an InP substrate, includes also an InGaAs layer which is meant to be sacrificial. The InP substrate is eliminated by selective wet etching (HCl solution). The sacrificial InGaAs layer is finally etched off by selective wet etching (FeCl₃ solution). The fabrication of the PC is then conducted using e-beam lithography [1].

4 HETEROGENEOUS ACTIVE/PASSIVE III-V/SILICON PHOTONIC DEVICE INTEGRATION: EXAMPLES OF RECENT ACHIEVEMENTS

4.1 Heterogeneous integration of microdisk lasers on silicon strip waveguides

Compact optical links for intra-chip optical interconnects are among the first recent developments where photonics is combined to microelectronics at the chip scale. In this context, impressive demonstrations of III-V / silicon heterogeneous integration along the refractive optical confinement scheme have been reported in the recent period. The group at Santa Barbara University associated with INTEL, have reported on the fabrication of a hybrid III-V / silicon photonic building block, where the heterogeneous integration lies within the device itself and which can be used for a variety of photonic components, laser, modulator, optical amplifier. These components operate in the wave-guiding regime and exhibit a wide optical bandwidth, at the expense of a rather large lateral size (see [8] for example). The European Community consortium in the frame of the FP6 PICMOS STREP project, has demonstrated III-V / silicon optical links including a III-V micro-disk laser and a III-V micro-detector evanescently coupled to a silicon micro-guide: unlike the US approach, it is chosen a compact solution for the optical micro-source [9, 10]. As shown in Figure 5, the electrically pumped laser micro-source is vertically linked by evanescent coupling to a silicon micro-strip waveguide, formed in a SOI substrate and separated from the micro-disk by a silica coupling-bonding interlayer. 3D FDTD simulation is used for the design of the structure.

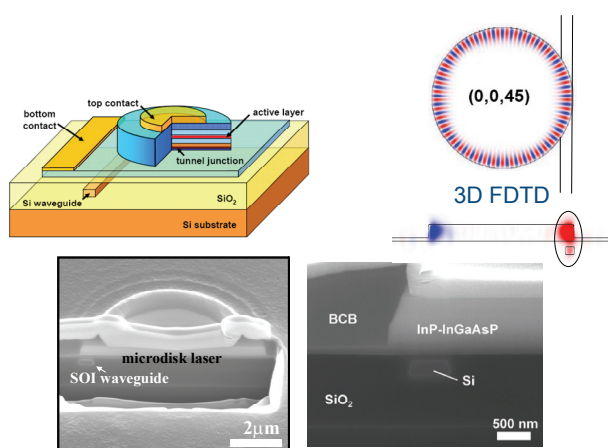


FIG. 5 Heterogeneous integration of a micro-disk laser with a silicon micro-strip waveguide. Evanescent coupling of the micro-source with the micro-guide is modeled using 3D FDTD simulation.

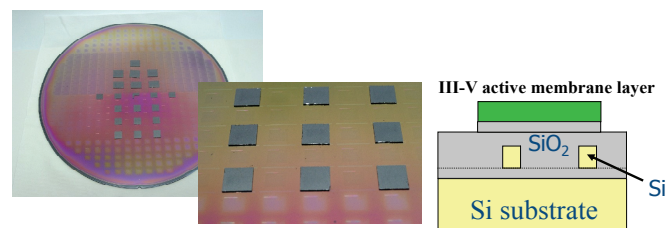


FIG. 6 Die to wafer bonding procedure.

Bonding of the III-V heterostructure membrane layers is achieved on top of the silicon photonic layer and restricted to the areas where it is needed, along the so called die to wafer bonding procedure (see Figure 6).

The technological procedure is described in detail in [10]. The laser emits at 1.6 μm , with a threshold current as low as 0.5 mA under continuous-wave operation at room temperature, and a threshold voltage of 1.65 V. The SOI-coupled laser slope efficiency was estimated to be 30 $\mu\text{W}/\text{mA}$, with a maximum unidirectional output power of 10 μW .

4.2 Heterogeneous integration of 2D photonic crystal membrane micro-lasers on silicon

The demonstration of a variety of micro-lasers based on photonic crystals has been reported in the international literature, following the pioneering work of the group at Caltech published in 1999, which concerned the production of the first micro-cavity laser (H₁ type), formed in an InP suspended membrane [11].

Let us remind that, in general, the lateral confinement of photons can be achieved in a 2D PC, either by trapping them in a localized defect or micro-cavity giving rise to a localized mode within a photonic band gap, or by slowing them down in a slow Bloch mode at an extreme of the dispersion characteristics. Those two approaches result in two classes of lasers, micro-cavity lasers and Bloch mode lasers. In the Bloch mode laser class two types of devices can be distinguished:

- Lasers designed for in plane emission: the operation point coincides with an extreme located below the light line.
- Lasers designed for surface emission, that is to say in free space: the operation point coincides with an extreme located above the light line.

The heterogeneous integration and demonstration of these different families of PC membrane lasers on silicon using InP active membrane molecular bonded on silica/silicon substrate has been pioneered by the group at Ecole Centrale de Lyon, in collaboration with CEA-LETI [1]-[3]. Figure 7 shows these different types of lasers, from the point of view of their operation points on the dispersion characteristics. Very low threshold power could be achieved (down to around 100 μW).

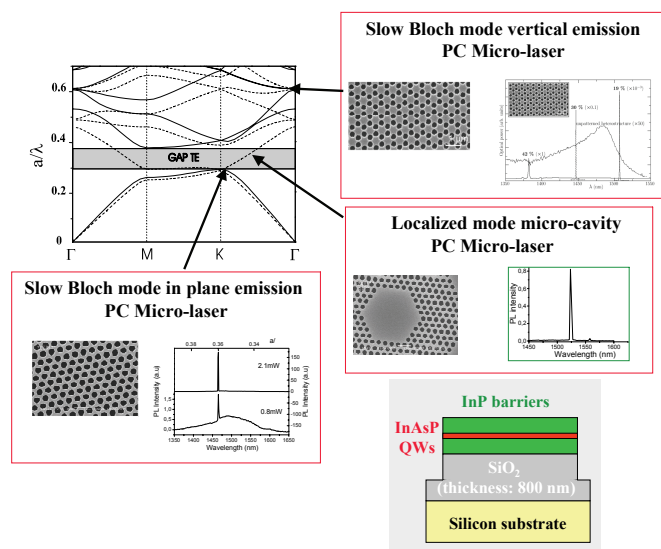


FIG. 7 Different families of PC membrane micro-lasers heterogeneously integrated on silicon.

5 CONCLUSION

It is hoped that the reader will have been convinced that nanometer scale heterogeneous III-V semiconductor-silicon photonic integration holds a very strong potential of innovation for micro-nano-photonics and pave the way to new developments for microelectronics. It has been emphasized in the present contribution that high optical index contrast micro-nano-photonics along the so-called semiconductor membrane approach and combining efficient refractive and photonic crystal optical confinement schemes have already proven convincing demonstrations of its ability to generate, in the short run, a wide range of photonic devices, combining compactness, spatial and spectral resolution, and whose fabrication meets the standards of the planar technology, familiar to the world of microelectronics. In brief micro-nano-photonics and microelectronics should be intimately associated for their mutual benefits: the former providing new functionalities missing to the latter, the latter offering its formidable technological efficiency to the former. III-V/Silicon heterogeneous integration technologies are expected to push efficiently this association, until it is strongly pulled by the market.

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